This Listing of Claims will replace all prior versions and Listings of Claims in the application:

**Listing of Claims:**

1. (Previously Canceled).

2. (Canceled).

3-8. (Previously Canceled).

9. (Previously Amended Two Times) A current mirror circuit comprising:

a current source;

a first PMOS transistor having a gate, a drain coupled to the gate and the current source, and a source coupled to a first power source, the gate of the first PMOS transistor applied a voltage $V_{g1}$;

a second PMOS transistor having a gate coupled to the gate of the first PMOS transistor, a drain coupled to a node, and a source coupled to the first power source, a mirror current flowing into the drain of the second PMOS transistor, the mirror current corresponding to the current source; and

a compensation circuit comprising:

at least one compensation PMOS transistor, each compensation PMOS transistor having a gate, a source coupled to the first power source, and a drain coupled to the node; and

at least one subtracter coupled to the drain of the first PMOS transistor and the second PMOS transistor, each subtracter configured to supply a voltage which is higher than the voltage $V_{g1}$ to the gate-source of each compensation PMOS transistor.

10. (Previously Amended One Time) The current mirror circuit according to claim 9, wherein the compensation PMOS transistor has a gate length and a channel width, respectively, equal to those of the second PMOS transistor.

11. (Previously Amended One Time) The current mirror circuit according to claim 9, wherein each of the subtracters supplies a voltage expressed by an arithmetic series $a_k$ to the gate-source of the at least one compensation PMOS transistor respectively, where $a_k$ is the arithmetic series equal to:

$V_{g1} - kV_{d1}$ (k = 1, 2, ...,n), wherein

$V_{d1}$ is the drain-source voltage of the second transistor,

$V_{g1}$ is the gate-source voltage of the second transistor, and

n is the number of PMOS transistors of the compensation circuit.

12-16. (Previously Canceled).

17. (Previously Amended Two Times) A current mirror circuit comprising:

a current source;

a first group of PMOS transistors connected in series, the first group of PMOS transistors including:

a first PMOS transistor having a gate, a drain coupled to the gate, and a source, wherein the source of the first PMOS transistor is coupled to a first power source, wherein the first PMOS transistor is defined as being electrically closest to the first power source in the first group of PMOS transistors, and

a second PMOS transistor having a gate, a drain coupled to the gate, and a source, wherein the drain of the second PMOS transistor is coupled to the current source,

wherein the second PMOS transistor is defined as being electrically closest to the current source in the first group of PMOS transistors;

a second group of PMOS transistors connected in series, wherein the number of PMOS transistors in the second group of PMOS transistors is equal to the number of PMOS transistors in the first group of PMOS transistors, the second group of PMOS transistors including:

a third PMOS transistor having a gate coupled to the gate of the first PMOS transistor, a drain, and a source, wherein the source of the third PMOS transistor is coupled to the first power

source, wherein the third PMOS transistor is defined as being electrically closest to the first power source in the second group of PMOS transistors, and

a fourth PMOS transistor having a gate coupled to the gate of the second PMOS transistor, a source, and a drain, wherein the fourth PMOS transistor is defined as being electrically furthest from the first power source in the second group of PMOS transistors;

a compensation circuit comprising a third group of PMOS transistors connected in series, wherein the number of PMOS transistors in the third group of PMOS transistors is equal to the number of PMOS transistors in the second group of PMOS transistors, the third group of PMOS transistors including:

a fifth PMOS transistor having a gate, a source, and a drain, wherein the source of the fifth PMOS transistor is coupled to the first power source, wherein the fifth PMOS transistor is defined as being electrically closest to the first power source in the third group of PMOS transistors, and

a sixth PMOS transistor having a gate, a source, and a drain, wherein the drain of the sixth PMOS transistor is coupled to the drain of the fourth PMOS transistor, wherein the sixth PMOS transistor is defined as being electrically furthest from the first power source in the third group of PMOS transistors; and

a group of subtracters, including:

a first subtracter coupled to the drain of the first PMOS transistor, the source of the third PMOS transistor, and the gate of the fifth PMOS transistor, the first subtracter configured to supply a difference voltage between a gate-source voltage and a drain-source voltage of the third PMOS transistor to the gate of the fifth PMOS transistor, and

a second subtractor coupled to the drain of the second PMOS transistor, the source of the fourth PMOS transistor and the gate of the sixth PMOS transistor, the second subtractor configured to supply a difference voltage between a gate-source voltage and a drain-source voltage of the fourth PMOS transistor to the gate of the sixth PMOS transistor.

18. (Previously Canceled).

19. (Cancelled).

20. (Previously Canceled).

21. (Cancelled).

22. (Canceled).